Amendments to the Specification

Please amend the specification by inserting after the title:

RELATED APPLICATION

This application is a divisional of U.S. Patent Application No. 09/264,672 filed on March 9, 1999, which is hereby incorporated by reference in its entirety. Priority under 35 U.S.C. §§120 and 121 is hereby claimed for benefit of the filing date of U.S. Patent Application No. 09/264,672.

Please amend the paragraph beginning at page 34, line 26, to read as follows:

The column address counter 30 generates a clock signal cacpz as soon as the write/read control signal from the command decoder 18 is input, and in response to the clock signal cacpz, the address generates section ~~34~~ 514 inputs the column address A0-An output by the address buffer/register & bank select 20. Along with this, a burst counter 504 generates a burst period signal endz to start a burst operation, and a clock generator 502 generates a clock signal intpz in response to a burst length in synchronization with the rising edge of the clock signal CLKO°. On the basis of the clock signal intpz, clock signals intp12z and intp0z are generated, and the column address is counted up at an address generating section 514 by these clock signal intp12z and intp0z to generate sequential addresses. Thus, the column address counter 30, on the basis of the burst length set at the mode register 28, the number of the column addresses having the number of data which is sequentially input or output are generated at every predetermined clock to be supplied to the banks 0 and 1.

Please amend the paragraph beginning at page 35, line 11, to read as follows:

In Fig.7, the clock signal CLKO° generated at the clock buffer 16 inputs to the clock generator 502 provided at a clock generating section 500 in the column address counter 30. Further, the write/read control signal from the command decoder 18 and the burst period signal endz from the burst counter 504 are input at the clock generator 502. The clock generator 502 outputs the clock cacpz for reading the external address and the clock signal intpz for generating the clock signal (intp0z and intp12z) for counting up in the internal generating address. The clock signal intpz output from the clock generator 502 inputs to the 1/2-frequency divider 506, on terminal B of a two-input switching switch 510 in a clock switch section 508, and one input terminal of a two-input AND circuit 512 in the clock section 508. The 1/2-frequency divider 506 generates a signal having a cycle twice as long as the clock signal intpz and then outputs to the other terminal A of the switching switch 510. The switching switch 510, on the basis of the level of the DDR signal from the mode register 28, switches the clock signal intpz and the signal having a cycle twice as long as the clock signal intpz. The switching switch 510 selects the terminal A when operating the SDRAM 1 in the SDR mode and the terminal B when operating the SDRAM 1 in the DDR mode. The signal selected by switching is input to an address generation section (A1, A2) 142 in the address generation section 514 as the clock signal intp12z. A signal which has reversed the DDR signal is input to the AND circuit 512 in the clock switch

section 508, outputting the clock signal intp0z to an address generating section (A0) 140 on the basis of the level of the DDR signal.